In the Claims:

13. (Original) A phase-change memory comprising:

a first electrode contact;

a phase-change layer on the first electrode contact; and

a second electrode contact on the phase-change layer, wherein a set state is a state in which amorphous nuclei are formed in the phase-change layer that has a set resistance of from about 4 kΩ to 6 kΩ, and a reset state is a state in which the number and density of the amorphous nuclei are greater than in the set state and has a reset resistance of about 6 kΩ to 20 kΩ.

14. (Previously Presented) The phase-change memory of Claim 13, wherein a current for writing the reset state and/or the set state on the phase-change layer is from about 10 μA to about 200 μA, and a period required for writing the reset state and/or the set state from the phase-change layer is from about 10 nanoseconds to about 100 nanoseconds.

15. (Previously Presented) The phase-change memory of Claim 13, wherein a current for writing the set state in the phase-change layer is from about 30 μA to about 50 μA, and a current for writing the reset state in the phase-change layer is from about 60 μA to about 200 μA.

16. (Previously Presented) The phase-change memory of Claim 13, wherein a diameter of the first electrode contact to which the current is applied to write the reset and set states in the phase-change layer is from about 40 nanometers to about 70 nanometers.

17. (Previously Presented) The phase-change memory of Claim 13, wherein a rising time and a falling time for writing the reset state and/or the set state in the phase-change layer is from about 1 nanosecond to about 4 nanoseconds.

18. (Previously Presented) The phase-change memory of Claim 13, wherein a current for reading the reset state and/or the set state is from about 3 μA to about 6 μA, and

a time required for reading the reset state and/or the set state is from about 5 nanoseconds to about 10 nanoseconds.

19. (Currently Amended) The phase-change memory of Claim 14, wherein a current for reading the reset state and/or the set state [iss]<u>is</u> from about 3 μA to about 6 μA, and a time required for reading the reset state and/or the set state is from 5 nanoseconds to about 10 nanoseconds.

26. (Original) A phase change memory, comprising:

first and second electrode contacts;

a phase-change layer between the first and second electrode contacts, the phase change layer providing a first state established by a first number of amorphous nuclei in a crystalline matrix in a region adjacent an interface between the phase-change layer and the first electrode.

27. (Original) The phase change memory of Claim 26, wherein the phase change layer further provides a second state established by a second number of amorphous nuclei in a crystalline matrix in the region adjacent the interface between the phase-change layer and the first electrode, the second number being greater than the first number.

28. (Original) The phase change memory of Claim 27, wherein the first number of amorphous nuclei and the second number of amorphous nuclei provide a ratio of resistances of the phase-change layer of from about 1.5 to about 3.

29. (Previously Presented) The phase change memory of Claim 27, wherein the first state of the phase-change layer provides a resistance of the phase-change layer of from about 4 to about 6 kΩ and the second state the phase-change layer provides a resistance of the phase-change layer of from about 6 to about 20 kΩ.

30. (Previously Presented) The phase change memory of Claim 27, wherein a current for writing the first state or the second state on the phase-change layer is from about

10 μA to about 200 μA, and a period required for writing the first state or the second state from the phase-change layer is from about 10 nanoseconds to about 100 nanoseconds.

31. (Previously Presented) The phase change memory of Claim 27, wherein a current required for writing the first state in the phase-change layer is from about 30 μA to about 50 μA, and a current required for writing the second state in the phase-change layer is from about 60 μA to about 200 μA.

32. (Previously Presented) The phase change memory of Claim 27, wherein a diameter of the first electrode contact to which a current is applied to write the first and second states in the phase-change layer is from about 40 nanometers to about 70 nanometers.

33. (Previously Presented) The phase change memory of Claim 27, wherein a current for reading the first state and/or the second state is from about 3 μA to about 6 μA, and a time required for reading the first state and/or the second state is from about 5 nanoseconds to about 10 nanoseconds.

34. (Original) A method of operating a phase change memory, comprising: establishing logic states in a phase change memory by controlling amorphous nucleation in a crystalline matrix of a phase-changeable material.

35. (Currently Amended) The method of Claim 34, wherein a first logic state is established by a first number of amorphous nuclei in the crystalline matrix and a second logic state is established by a second number of amorphous nuclei in the crystalline matrix ~~in the~~, the second number being greater than the first number.

36. (Original) The method of Claim 35, wherein the first number of amorphous nuclei and the second number of amorphous nuclei provide a ratio of resistances of the phase-changeable material of from about 1.5 to about 3.

37. (Original) The method of Claim 35, wherein the first logic state provides a resistance of the phase-change layer of from about 4 kΩ to about 6 kΩ and the second logic state provides a resistance of the phase-change layer of from about 6 kΩ to about 20 kΩ.

38. (Original) The method of Claim 35, wherein controlling amorphous nucleation comprises controlling a current for writing the first logic state or the second logic state to be from about 10 μA to about 200 μA, and a period required for writing the first logic state or the second logic state to be from about 10 nanoseconds to about 100 nanoseconds.

39. (Original) The method of Claim 35, wherein controlling amorphous nucleation comprises:

controlling a current for writing the first logic state to be from about 30 μA to about 50 μA; and

controlling a current or writing the second logic state to be from about 60 μA to about 200 μA.

40. (Original) The method of Claim 35, wherein a diameter of the first electrode contact to which a current is applied to write the first and second logic states is from about 40 nanometers to about 70 nanometers.

41. (Original) The method of Claim 35, further comprising controlling a current for reading the first logic state and/or the second logic state to be from about 3 μA to about 6 μA, and a time for reading the first state and/or the second state to be from about 5 nanoseconds to about 10 nanoseconds